Reliability Analysis of SnPb and SnAgCu Solder Joints in FC-BGA Packages with Thermal Enabling Preload

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Abstract

Modern semiconductor devices in many applications require a thermal solution to remove the heat away from the device and maintain a certain operating temperature. These thermal solutions typically use a heat sink and a thermal interface material (e.g. thermal grease) between the device and the heat sink. A compressive load is applied to reduce the thermal resistance of the interface and facilitate better heat transfer from the device to heat sink. Depending on the magnitude, this compressive preload may affect the fatigue behavior of second level solder joints connecting the device to PCB in a thermal cycling environment. This paper describes the experimental setup and test results to evaluate the reliability of solder joints in the presence of a preload. 3-D nonlinear finite element analysis is performed to simulate the effect of compressive load in thermal cycling. Both SnPb and SnAgCu solder alloys are studied with various levels of preload.

Introduction

Higher performance, feature integration, and new applications for semiconductor devices require high efficiency thermal solutions to remove the power dissipated and maintain the device operating temperature. A common thermal solution uses a heat sink and a thermal interface material between the electronic package and the heat sink. In order to reduce the thermal resistance at the interface, a compressive load is maintained between the package and the heat sink, via a heat sink spring clip or similar means. This compressive preload affects the deformation behavior of the package/board assembly in a thermal cycling environment, which, in the absence of this preload, is controlled only by the coefficient of thermal expansion (CTE) mismatch between the package and the board. Therefore predicting the low-cycle fatigue life of solder joints in preloaded electronic packages has remained a challenge.

Experimental data for Flip-Chip Ball Grid Array (FC-BGA) packages shows that solder joint fatigue life and failure location can change when a preload is applied [1][2]. This paper describes the experimental setup which simulates the thermal preload during reliability testing. Test data for BGA packages under different levels of preload during thermal cycling is presented. 3-D nonlinear finite element analysis is performed to simulate the behavior of solder joints for SnPb and SnAgCu alloys. Unlike conventional solder joint finite element analysis without a preload, which requires only 2-3 thermal cycles to achieve a stabilized cyclic solution [3], preload simulation requires more cycles to reach a relatively stable cyclic pattern. The paper will investigate when this stable pattern can be reached in the presence of a preload. The effect of board size will be studied as board dimensions (length & width) used in the finite element model will have an impact on the results. SnPb and SnAgCu solder joints respond differently to preload, which will be discussed in detail.

Experimental Setup

A generic loading fixture has been developed to experimentally evaluate the effect of compressive preload [1][2] on FC-BGA packages with exposed silicon die as shown in Figure 1. The loading fixture consists of a top loading plate made of aluminum. The top plate is used to compress a low stiffness spring on top of the FC-BGA package. The use of low stiffness spring can make sure the creep deformation of the package will not alter the magnitude of the applied compressive load. An aluminum disk is placed between the spring and package to mechanically simulate the heat sink. Thermal interface material is applied between the aluminum disk and the package. The top plate is bolted to the circuit board in a square pattern near the corners of the FC-BGA package. To simulate commonly used stamped metal or bent wire heat sink clips, the fixture is configured in a way such that the board is allowed to deflect between the four support points. To minimize over-constraining the board, dome washers are used to support the board on the bottom side, as seen in Figure 1.

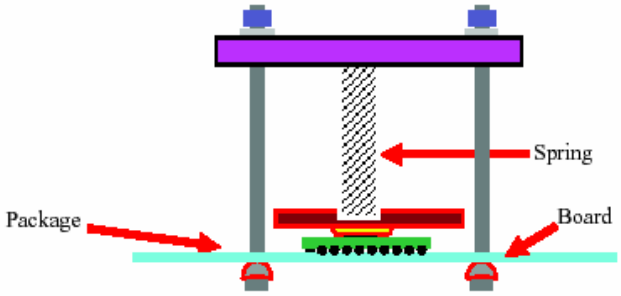


Figure 1: Compression loading test fixture [2]

The load is applied to the fixture by means of a hydraulic load frame. The fixture is placed in the frame with a plate supporting the bottom of the fixture. The desired compressive load is applied to the top plate with the upper hydraulic cross head. The nuts on the four bolts of the fixture are then tightened until 50% of the load has been removed from the load frame load cell. Then the hydraulic load frame cross head is moved away from the fixture.

The loaded fixtures are placed in thermal cycling chambers. Although efforts were made to minimize the thermal mass of the fixture, use of the fixture still adversely affects the chamber capacity. The component temperatures are brought to conform to accelerated test specification by adjusting the chamber profile.

At each thermal cycle read-out, electrical continuity and dye & peel analysis are conducted to monitor the fatigue

performance of solder joints. The test package and board design ensures that all solder joints in critical areas can be fully tested electrically. The dye & peel analysis provides an accurate measurement of solder joint crack area.

Experiment Results

FC-BGA test data with preload has been reported in [2]. The crack area as percentage of total solder joint area is plotted in Figure 2. It can be seen that the solder joint crack % area under the die region is relatively higher than at package corner when there is no preload is applied. This shows that critical solder joint is under the die region.

When compressive preload is increased to normalized value of 0.5, solder joint crack % area under the die region and at the package corner become comparable. This load is considered as the transition point where the critical solder joint location starts to switch from under the die region to the package corner. SnPb and SnAgCu solder undergo this transition at different load levels.

As compressive load is further increased to a normalized value of 1, data shows that solder joint cracking at package corner is higher than the die region. Hence, the risk is now dominated by the package corner solder joint failure.

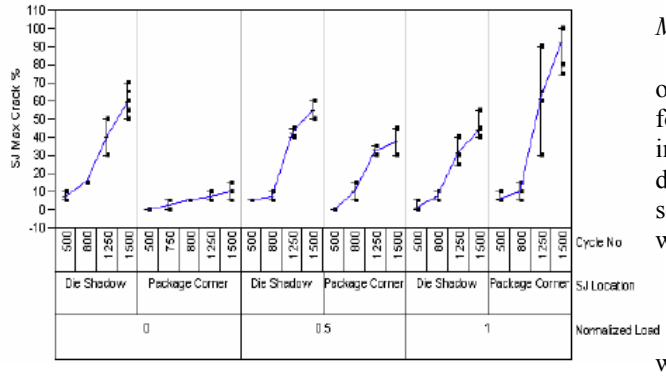


Figure 2: Effect of preload on critical solder joint location [2]

Modeling Approach

A typical FC-BGA package is modeled with finite element method using commercially available software ABAQUS and is shown in Figure 3.

A quarter of the package is simulated due to symmetry. 3D linear hexahedral element with reduced-integration (C3D8R) is used to increase the computational efficiency without a significant loss of accuracy [3]. The model includes the silicon die, an underfill layer, the BGA substrate, the PCB, and solder joints with copper pads on both BGA substrate and PCB interfaces. The solder joints are solder mask defined (SMD) on the BGA substrate side and metal defined (MD) on the PCB side. Two different mesh density patterns are used to model the solder joints as shown in Figure 4. The critical solder joints under the die shadow corner and at the package corner use a refined mesh pattern (Figure 3). The refined solder joint mesh includes a 25 micron thick region (with 2 layers of elements) at each solder/copper pad interface. The stresses and strains are volumetrically averaged in these 2 regions to overcome the edge stress singularity at the solder to copper pad interfaces [4].

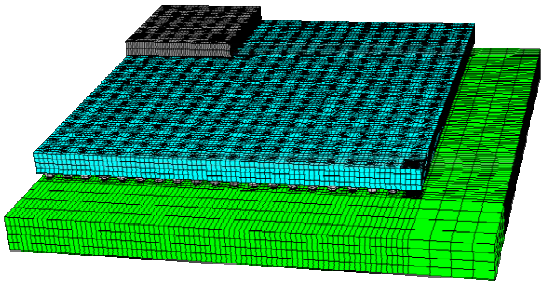


Figure 3: Finite element model

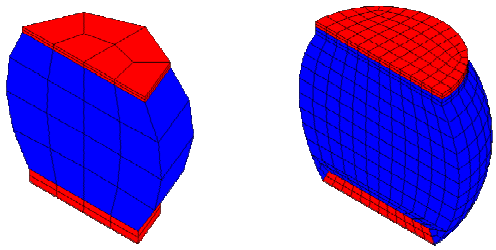


Figure 4: Details of solder ball coarse and refined mesh density patterns

Material Properties

A creep model that captures the total strain behavior in the operating range was proposed by Wong, Helling, and Clark for 63Sn37Pb eutectic alloy [6]. Bhatti et al. [7][8][9] implemented this constitutive model and developed 3-dimensional package level finite element models to perform solder joint creep simulations. This material model can be written as:

$$\dot{\varepsilon} = \frac{\dot{\sigma}}{E} + B_1 D\left(\frac{\sigma}{E}\right)^3 + B_2 D\left(\frac{\sigma}{E}\right)^7 \quad (1)$$

where $\dot{\varepsilon}$ is the total strain rate and σ is the stress. B_1 = $1.7\text{x}10^{12}$/Sec and B_2 = $8.9\text{x}10^{24}$/Sec. D and modulus of elasticity E are temperature dependent:

$$D = \exp\left(\frac{-5413}{T}\right)$$

$$E(MPa) = 56000 - 88 \times T$$

T is absolute temperature in K.

The creep model for SnAgCu lead free solder has a similar form, as shown in equation (2) [10]:

$$\dot{\varepsilon} = \frac{\dot{\sigma}}{E} + A_1 D_1\left(\frac{\sigma}{\sigma_n}\right)^3 + A_2 D_2\left(\frac{\sigma}{\sigma_n}\right)^{12} \quad (2)$$

$$D_1 = \exp\left(\frac{-3223}{T}\right),\ D_2 = \exp\left(\frac{-7348}{T}\right)$$

$$E(MPa) = 59533 - 66.667 \times T$$

The constants used in the equations are: $A_1 = 4.0\text{x}10^{-7}$/Sec and $A_2 = 1.0\text{x}10^{-12}$/Sec. σ_n=1MPa.

Published material properties [3] are used for all other materials as listed in Table 1.

Loading Condition

In the simulation, preload is applied as a uniform pressure on top of the silicon die. A single node on the bottom of PCB

where the support point is located is constrained in the vertical direction to simulate the fixture setup described in Figure 1. Three normalized preloads are investigated: 0 (no-preload), 0.5, and 1.0.

Thermal cycle range studied in the paper is -25 to 100°C. The dwell time is 15 minutes for both high and low temperatures, and the ramp up & down time is 8 minutes each. The total cycle time is 43 minutes. The preload is ramped up during a 1 minute interval at 100°C (to accelerate creep/stress relaxation at room temperature storage) and then thermal cycle loading is applied.

Table 1 Material Properties

Material	Young's Modulus (GPa)	Poisson's Ratio	Coefficient of Thermal Expansion (ppm/°C)
Silicon	131.0	0.3	2.6
Copper	128.7	0.3435	17.0
Underfill	9.9	0.23	24.0
Substrate	22.0	0.11	17.0
PCB	24.2	0.11	19.6
SnPb			25.5
SnAgCu			20.0

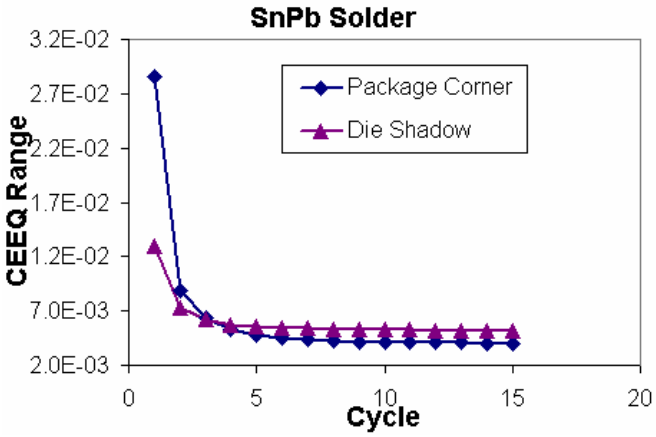


Figure 5: Averaged per-cycle CEEQ of SnPb solder with normalized preload of 1.0

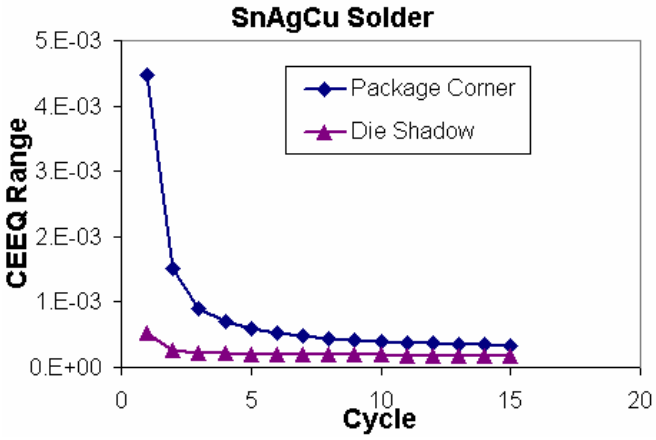


Figure 6: Averaged per-cycle CEEQ of SnAgCu solder with normalized preload of 1.0

Investigation of Stabilized Results with Preload

Solder joint simulation without preload requires only 2-3 cycles to achieve a stabilized cyclic pattern [3], which means that parameters such accumulated creep strain (CEEQ) *per-cycle* reach a constant value. However, when a preload is applied to the structure in addition to thermal cycling, solder joints will continue to creep under the constant preload. Hence, theoretically speaking, the structure may never reach stabilized cyclic pattern. In reality, solder joints creep significantly due to preload in the beginning after the load is applied. After some time, the incremental creep per cycle due to preload does not change much, and thus a relatively stable cyclic pattern can still be reached. Figure 5 shows the per-cycle CEEQ for SnPb solder joints under the die shadow corner and at package corner for 15 cycles under a normalized load of 1.0. In the first cycle, the per-cycle CEEQ at the package corner is much higher that under the die shadow corner. As thermal cycling continues, the per-cycle CEEQ at package corner falls below that under the die shadow corner. Both locations reach relatively stable per-cycle CEEQ values in 15 cycles.

Figure 6 shows the per-cycle CEEQ for SnAgCu solder joints under the normalized load of 1. Once again, it can be seen that relatively stabilized values are reached in 15 cycles. The package corner solder joint always has higher per-cycle CEEQ than the die shadow location.

Previous studies have used total CEEQ value at the end of the third cycle [1] to make comparison between the package corner and die shadow corner solder joints. This information could be misleading for SnPb as seen by the cross-over point in Figure 5. As seen in Figures 5 and 6, more simulation cycles are needed to make the right conclusion when a preload is applied.

PCB Board Size Effect

When performing solder joint simulations without preload, the PCB dimensions (length and width) in the model are usually same as the package length and width [3]. When a preload is applied, we have two options in setting the PCB dimensions in the model. The first option is to use the support span as PCB dimensions and ignore the board outside the support region. This is referred to as 'small board' in the following discussion and the model is shown in Figure 3. Second option is to use the actual PCB dimensions (a test board in this case). This is referred to as the 'big board' option, as shown in Figure 7. Since in preload condition, the bending deformation dominates the solder joint behavior at the package corner, it is important to investigate the effect of PCB size in the model.

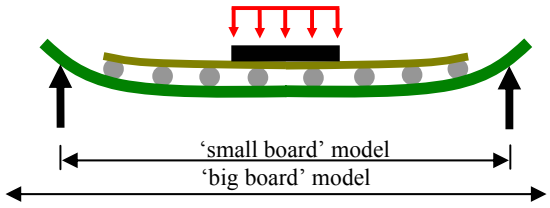


Figure 7: Illustration of modeling board size effect

Figures 8 and 9 show the effect of PCB size on per-cycle CEEQ at die shadow corner and package corner locations for SnPb and SnAgCu, respectively, for no preload case. The results show that the board size has a relatively small effect on the per-cycle CEEQ at the die shadow corner. However, the per-cycle CEEQ at the package corner is significantly higher when larger PCB size is used. In particular, the per-cycle CEEQ for SnAgCu shows a dramatic difference between the two different PCB sizes. As mentioned earlier, solder joints near the package corner experience deformation mainly controlled by PCB bending caused by the combined effect of CTE mismatch and preload. Therefore the PCB size affects the local bending behavior at the package corner greatly. Because the SnAgCu is stiffer and more creep-resistant, it is more sensitive to PCB size than SnPb.

In the subsequent analysis in this paper, all results are based on the actual test board size in the model.

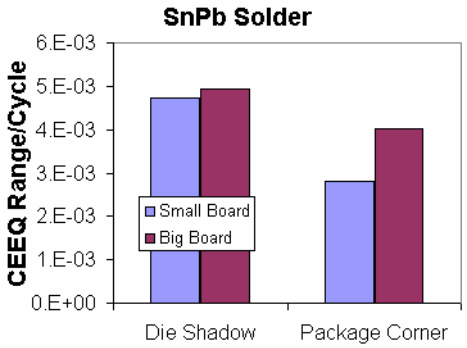


Figure 8: Comparison of per-cycle CEEQ for different board sizes, SnPb solder

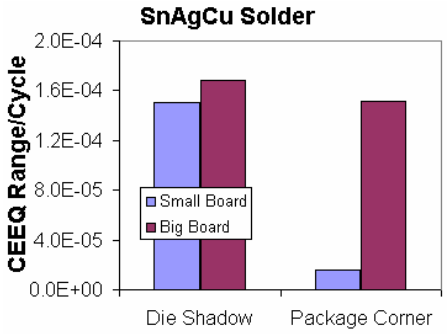


Figure 9: Comparison of per-cycle CEEQ for different board sizes, SnAgCu solder

Results and Discussions

In this section, the simulation results with preload are presented and discussed for SnPb and SnAgCu solders.

SnPb Solder Alloy

The per-cycle CEEQ for solder joints at package corner and die shadow corner are plotted in Figures 10 and 11, respectively, under 3 normalized preload conditions (0, 0.5 and 1). Interestingly, the stabilized value of per-cycle CEEQ seems insensitive to the preload level at both the package corner and the die shadow corner. In other words, in the simulated range, the preload has no significant effect on the per-cycle CEEQ for SnPb alloys. Figure 12 compares the per-cycle CEEQ at the two locations as a function of preload. It can be seen that per-cycle CEEQ at the die shadow corner is consistently higher than at the package corner, and further confirms that the effect of preload on per cycle CEEQ is insignificant.

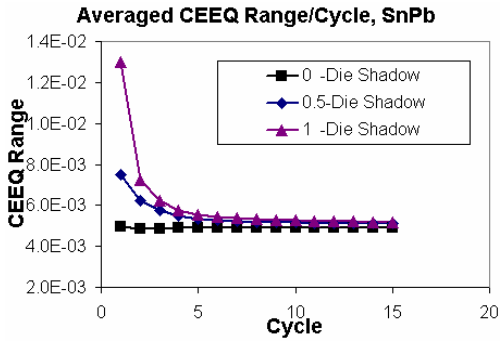


Figure 10: Averaged per-cycle CEEQ at die shadow

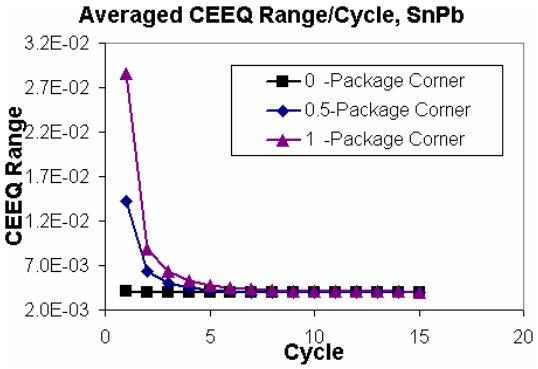


Figure 11: Averaged per-cycle CEEQ at package corner

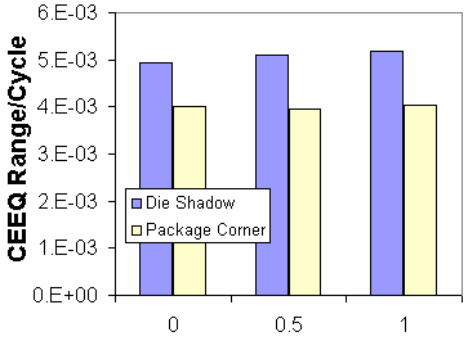
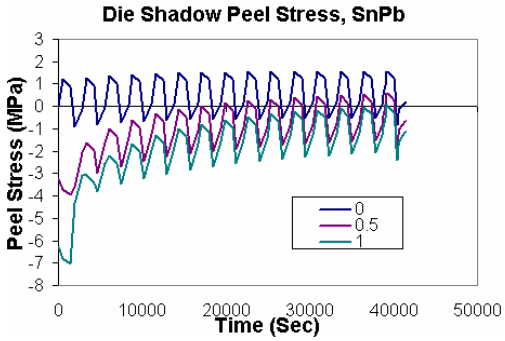


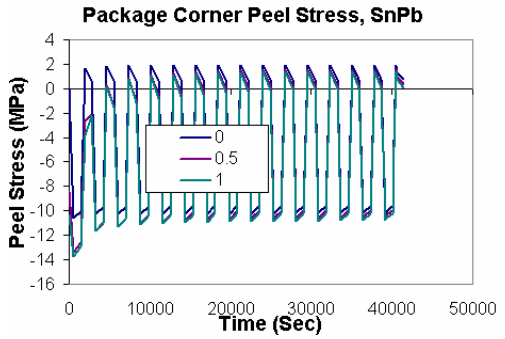
Figure 12: Comparison of steady-state per-cycle CEEQ with different preload levels

'Peel' stress in solder joints is also volumetrically averaged in 2 thin solder layers at the solder to copper pad interfaces described earlier. The peel stress is defined as the stress normal to the solder / copper pad interface. The history of peel stress is shown in Figure 13(a) and (b) for solder joints under the die shadow corner and at the package corner, respectively. These graphs show that, at the die shadow corner, the peel stress becomes more compressive with increasing preload. However, peel stress at the package corner does not seem to change much with the preload. This implies that the solder joint crack growth rate at the die shadow corner will be slower as the preload is increased, because of a more compressive peel stress and the per-cycle CEEQ remains almost unchanged. As a result, the failure location is likely to

shift from under the die shadow corner to the package corner. This observation is in agreement with the experimental results described in the previous section.



(a) Corner of die shadow



(b) Package corner

Figure 13: Peel stress history for SnPb solder

SnAgCu Solder Alloy

Package with SnAgCu solder joints exhibits a different deformation behavior compared to SnPb. Figure 14 and Figure 15 show the per-cycle CEEQ for the solder joint under the die shadow corner and at the package corner, respectively. It can be seen that, compared to SnPb, SnAgCu requires more cycles to reach a relatively stabilized state. Figure 16 compares the stabilized per-cycle CEEQ at the two locations for different preload conditions. In contrast to the SnPb behavior, the per-cycle CEEQ at the package corner for SnAgCu increases significantly with the increasing preload. Similar to SnPb, the per-cycle CEEQ at the die shadow corner is not sensitive to the preload. Furthermore, per-cycle CEEQ is higher at the die shadow corner with no preload, but at 0.5 preload, package corner has higher per-cycle CEEQ. The gap becomes even larger at 1.0 preload, suggesting a potential shift in the failure location from die shadow corner to package corner when preload is increased. The experimental data is not conclusive whether this shift occurs for SnAgCu solder in the tested range of preload.

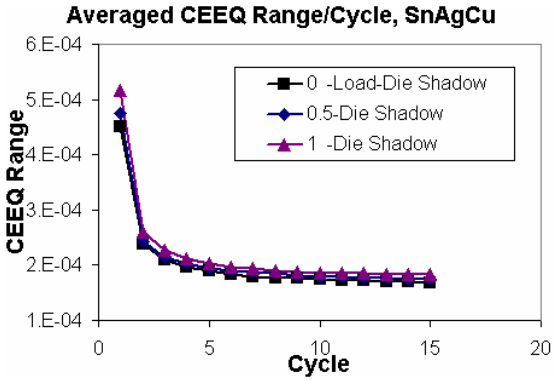


Figure 14: History of averaged per-cycle CEEQ at the corner of die shadow

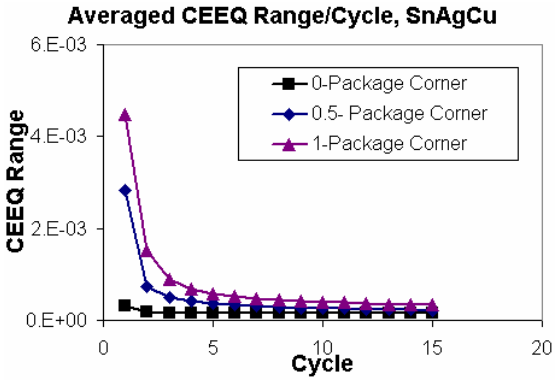


Figure 15: History of averaged per-cycle CEEQ at package corner

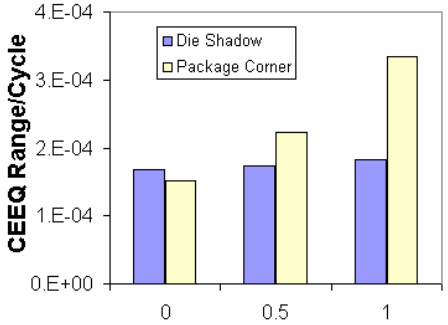


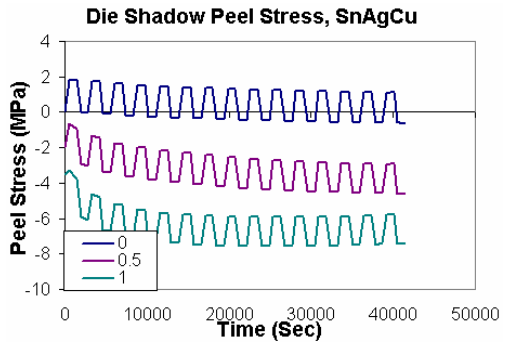
Figure 16: Comparison of steady-state per-cycle CEEQ with different preload levels

Averaged peel stress history of SnAgCu solder joints are shown in Figure 17 (a) and (b) for die shadow corner and package corner locations, respectively. Preload affects the peel stress at both locations, which is different from the SnPb behavior. Peel stress at both locations becomes more compressive with increasing preload.

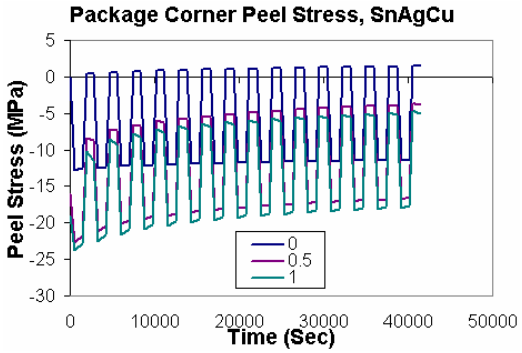
Discussion

The preload condition brings additional challenges to modeling fatigue behavior of solder joints. Traditional fatigue models have used accumulated solder creep strain or strain energy density as damage parameters to predict the number of cycles to failure. The results described in previous sections show that the peel stress state in the solder joint changes significantly when preload is applied. A tensile peel stress will facilitate crack growth, but a compressive stress tends to impede crack growth. This will affect the solder joint fatigue

life and can even change the failure location in the package. This analysis indicates that a more advanced fatigue law is needed for the preload case which accounts for both the conventionally used damage parameters (accumulated creep strain or strain energy per cycle) and the nature of peel stress in the solder joints. Such an enhanced model may even make life prediction for no preload case more accurate.



(a) Corner of die shadow



(b) Package corner

Figure 17: Peel stress history of SnAgCu solder

Summary

Empirical data shows that the existence of compressive preload on FC-BGA packages may cause a shift in the critical solder joint location from under the die shadow region to the package corner. Finite element analysis was performed to investigate the solder joint response to preload in a thermal cycling environment. Since preload is maintained throughout thermal cycling, an absolutely stable cyclic creep pattern may never be reached. However, simulations show that creep due to preload accumulates significantly only in the initial stage (a few cycles) after the preload is applied. After several cycles (~15), a relatively stable cyclic creep pattern emerges during thermal cycling. Therefore simulation results based on accumulated creep at the end of only a few cycles may lead to false conclusions. Analysis should be performed until a stable cyclic pattern is achieved and the stabilized per-cycle increment should be used for reliability assessment. Results also show that PCB length and width dimensions in the model have a significant impact on the solder joint behavior at the package corner, but not on the solder joints under the die shadow region.

SnPb and SnAgCu solders respond very differently with respect to the preload. For SnPb, the stabilized per-cycle creep strain accumulation does not change much with respect to the preload in the range considered in this paper. Although the solder joint under the die shadow corner has greater per-cycle CEEQ than at the package corner, more compressive stress is induced at die shadow corner when preload is increased. For SnAgCu, on the other hand, the per-cycle CEEQ at the package corner increases dramatically with the increase in preload, and at a certain preload, it will surpass the per-cycle CEEQ at the die shadow corner. The stress state becomes more compressive at both locations with increasing preload. A more advanced fatigue law formulation is needed to correctly predict failure location and fatigue life of solder joints in electronic packages under compressive preload and thermal cycling.

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